

ESHA CHOUKSE

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EDUCATION

University of Texas at Austin

Aug 2014 - present

Graduate student in Computer Architecture and Embedded Systems, Electrical Engineering

Indian Institute of Technology, Kharagpur

July 2008- Apr 2012

B.Tech(Hons.) in Electronics and Electrical Communication and Minor in Computer Science

EXPERIENCE

Intel

May 2017 - Aug 2017

Memory Architecture Intern

Hillsboro, OR

- Explored several opportunities to improve memory latency for server chips, resulting in several avenues for memory system optimization.

ARM

May 2016 - Aug 2016

Research Intern

Austin, TX

- Evaluated various metrics for using on-chip DRAM to alleviate the challenges with a non-volatile main memory system

ARM

May 2015 - Aug 2015

Verification Intern

Austin, TX

- Helped develop a new tool for ISA level testing in interesting multiprocessor scenarios
- Implemented various features like exception level switching and exception handling in the tool

Qualcomm

July 2012 - Aug 2014

Embedded Systems Engineer

Hyderabad, India and San Diego, CA

- Implemented Boot flow/ microcode for various Snapdragon chipsets (8974Pro, 8x26, 8x10, 9x35, 8916, 9x45, 8936).
- Worked closely with ARM cortex M3/A7/A15/A53, Qualcomm Krait, Hexagon processors.
- Was involved in Boot code deliverables, pre-silicon emulation/simulation and System-on-Dock testing.
- **Filed a patent** on NAND Flash Failsafe over-the-air upgrades. *US20140173187*
- Was awarded 8 Qualstars (Certificates of merit) within 2 years.

Mentor Graphics

May 2011 - July 2011

Summer Intern

Noida, India

- Worked on building the emulation platforms: Testbench Xpress and Veloce.
- Developed various libraries, most importantly for checkpoint restore functionality.

RESEARCH

Efficient OS-transparent Main Memory Compression

Research, UT Austin

Aug 2015 - Present

- An OS-transparent, hardware-only mechanism for main memory compression for storage benefits.
- Made optimizations to decrease the compression-related data movement.
- Used novel methodology for accurate and holistic evaluation of a compressed memory system.

- Submitted to ISCA 2018

Bit-Plane Compression

Research, UT Austin

Jan 2015 - Sep 2015

- Bandwidth savings in GPGPUs using Bit-plane compression over transformed data
- Published, ISCA 2016

TERM PROJECTS

Reinforcement Learning based driving simulation

Machine Learning Term Project, UT Austin

Jan 2017 - Apr 2017

- Used Q-Learning to train a simulated car in an environment with other cars, pedestrians, and traffic lights.

Health Radar Android App

Mobile Computing Term Project, UT Austin

Sep 2016 - Dec 2016

- Bluetooth Beacons based Android app for tracking and reporting exposure to diseases.

Microarchitecture: Cache and Memory design

Microarchitecture Term Project, UT Austin

Jan 2016 - Apr 2016

- Designed and implemented the memory subsystem for an x86 processor in structural verilog.
- Added features like MSHRs, Write-buffer, Victim-buffer, Critical Word First and Row Buffers.

Krispy Kache: Remote cache injection in multicore systems

Parallel Computer Architecture Term Project, UT Austin

Sep 2015 - Dec 2015

- Evaluated Software-based and Hardware-prediction based approaches to cache-block injection into remote-core's caches.

Parity Based Erasure Correction for Fused Data Structures

Distributed Systems Term Project, UT Austin

Sep 2015 - Dec 2015

- Implemented and evaluated EvenOdd, Replication and RS-encoding mechanisms in fused backups for servers.

Memory Aware Warp Scheduling in GPGPUs

Parallelism and Locality Term Project, UT Austin

Feb 2015 - Apr 2015

- Extended the idea of Large Warps to make scheduling decisions based on locality of thread accesses

Hourglass- Solving Distributed Priority Inversion

Real-time OS Term Project, UT Austin

Feb 2015 - Apr 2015

- Defined the problem of distributed priority inversion in a multi-process embedded system
- Solved the problem by implementing locks using a special, new OS construct
- Implemented in uCOS-III

Shared stack using Queue delegation and Elimination in a Multicore system

Multicore Computing Term Project, UT Austin

Sep 2014 - Dec 2014

- Implemented a fast shared stack using queue delegation and elimination

Architecture Design and FPGA implementation of Efficient Face Recognition

Senior Design Project, IIT Kharagpur

Sep 2011-Apr 2012

- Designed and implemented a time and computation efficient eigenface algorithm on Xilinx FPGA.

RELEVANT COURSES

- Parallelism and Locality
- Computer Architecture
- Distributed Systems
- Machine Learning
- Real time Operating Systems
- Dynamic Compilation
- Microarchitecture
- Compilers
- Parallel Computer Architecture
- Multicore Computing
- Mobile Computing

TECHNICAL STRENGTHS

Programming/Scripting	C, C++, Java, MPI, CUDA, Cilk, pThreads, python
Testing Platforms and simulators	Pin, Trace32, Veloce, GPGPUSim
Protocols	USB, PCIe, eMMC/SD, NAND, SPI, HSIC, NOCs
Processor Architectures	ARM Cortex A/M for v8, Hexagon, Intel x86