

# ESHA CHOUKSE

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## EDUCATION

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**University of Texas at Austin** *Aug 2014 - May 2019(expected)*  
PhD Candidate in Computer Architecture and Embedded Systems, Electrical Engineering  
*GPA: 4.0/4.0*

**Indian Institute of Technology, Kharagpur** *July 2008- Apr 2012*  
B.Tech(Hons.) in Electronics and Electrical Communication and Minor in Computer Science  
*GPA: Major: 8.8/10.0 Minor: 10.0/10.0*

## EXPERIENCE

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**NVIDIA Research** *May 2018 - Aug 2018*  
*Research Intern* *Austin, TX*

- Analyzed the data of various GPU workloads, and their entropy patterns.
- Designed a compressed memory system designed for the GPU model, which works well with a variety of workload-types of interest.

**Intel** *May 2017 - Aug 2017*  
*Memory Architecture Intern* *Hillsboro, OR*

- Explored several opportunities to improve memory latency for server chips, resulting in several avenues for memory system optimization.

**ARM** *May 2016 - Aug 2016*  
*Research Intern* *Austin, TX*

- Evaluated various metrics for using on-chip DRAM to alleviate the challenges with a non-volatile main memory system

**ARM** *May 2015 - Aug 2015*  
*Verification Intern* *Austin, TX*

- Helped develop a new tool for ISA level testing in interesting multiprocessor scenarios
- Implemented various features like exception level switching and exception handling in the tool

**Qualcomm** *July 2012 - Aug 2014*  
*Embedded Systems Engineer* *Hyderabad, India and San Diego, CA*

- Implemented Boot flow/ microcode for various Snapdragon chipsets (8974Pro, 8x26, 8x10, 9x35, 8916, 9x45, 8936).
- Worked closely with ARM cortex M3/A7/A15/A53, Qualcomm Krait, Hexagon processors.
- Was involved in Boot code deliverables, pre-silicon emulation/simulation and System-on-Dock testing.
- **Filed a patent** on NAND Flash Failsafe over-the-air upgrades. *US20140173187*
- Was awarded 8 Qualstars (Certificates of merit) within 2 years.

**Mentor Graphics** *May 2011 - July 2011*  
*Summer Intern* *Noida, India*

- Worked on building the emulation platforms: Testbench Xpress and Veloce.
- Developed various libraries, most importantly for checkpoint restore functionality.

## RESEARCH AND PUBLICATIONS

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### **SparseTrain: Reducing Training Time By Gradual Structural Pruning**

*Research, UT Austin*

*October 2018 - Present*

- Under review for **International Conference on Machine Learning (ICML) 2019** (2nd Author).

### **Reducing the context size of Object Detection Networks Using Compression**

*Research, UT Austin*

*December 2018 - Present*

- Ongoing work to increase the possible batch size per GPU for the ODNs.

### **Buddy Compression: Compressing Device Memory in GPUs**

*Research, NVIDIA Research and UT Austin*

*March 2018 - November 2018*

- Proposing a compressed data management well-suited to GPU applications, both, HPC and DL.
- Under review for **International Symposium on Computer Architecture (ISCA) 2019**.

### **Compresso: Efficient OS-transparent Main Memory Compression**

*Research, UT Austin*

*Aug 2016 - Dec 2017*

- An OS-transparent, hardware-only mechanism for main memory compression for storage benefits.
- Made optimizations to decrease the compression-related data movement.
- Used novel methodology for accurate and holistic evaluation of a compressed memory system.
- Published in **International Symposium on Microarchitecture (MICRO) 2018**.

### **CompressPoints: An Evaluation Methodology for Compressed Memory Systems**

*Research, UT Austin*

*Oct 2015 - Apr 2016*

- Methodology for choosing better representative regions of workloads for studies that require data-representativeness.
- Published in **IEEE Computer Architecture Letters (CAL)**, July-Dec 2018

### **Bit-Plane Compression**

*Research, UT Austin*

*Jan 2015 - Sep 2015*

- Bandwidth savings in GPGPUs using Bit-plane compression over transformed data
- Published in **International Symposium on Computer Architecture (ISCA) 2016**.

## TERM PROJECTS

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### **Reinforcement Learning based driving simulation**

*Machine Learning Term Project, UT Austin*

*Jan 2017 - Apr 2017*

- Used Q-Learning to train a simulated car in an environment with other cars, pedestrians, and traffic lights.

### **Health Radar Android App**

*Mobile Computing Term Project, UT Austin*

*Sep 2016 - Dec 2016*

- Bluetooth Beacons based Android app for tracking and reporting exposure to diseases.

### **Microarchitecture: Cache and Memory design**

*Microarchitecture Term Project, UT Austin*

*Jan 2016 - Apr 2016*

- Designed and implemented the memory subsystem for an x86 processor in structural verilog.
- Added features like MSHRs, Write-buffer, Victim-buffer, Critical Word First and Row Buffers.

### **Krispy Kache: Remote cache injection in multicore systems**

*Parallel Computer Architecture Term Project, UT Austin*

*Sep 2015 - Dec 2015*

- Evaluated Software-based and Hardware-prediction based approaches to cache-block injection into remote-core's caches.

### **Parity Based Erasure Correction for Fused Data Structures**

*Distributed Systems Term Project, UT Austin*

*Sep 2015 - Dec 2015*

- Implemented and evaluated EvenOdd, Replication and RS-encoding mechanisms in fused backups for servers.

### **Memory Aware Warp Scheduling in GPGPUs**

*Parallelism and Locality Term Project, UT Austin*

*Feb 2015 - Apr 2015*

- Extended the idea of Large Warps to make scheduling decisions based on locality of thread accesses

### **Hourglass- Solving Distributed Priority Inversion**

*Real-time OS Term Project, UT Austin*

*Feb 2015 - Apr 2015*

- Defined the problem of distributed priority inversion in a multi-process embedded system
- Solved the problem by implementing locks using a special, new OS construct
- Implemented in uCOS-III

### **Shared stack using Queue delegation and Elimination in a Multicore system**

*Multicore Computing Term Project, UT Austin*

*Sep 2014 - Dec 2014*

- Implemented a fast shared stack using queue delegation and elimination

### **Architecture Design and FPGA implementation of Efficient Face Recognition**

*Senior Design Project, IIT Kharagpur*

*Sep 2011-Apr 2012*

- Designed and implemented a time and computation efficient eigenface algorithm on Xilinx FPGA.

## **RELEVANT COURSES**

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|----------------------------|-------------------------------|----------------------------------|
| - Parallelism and Locality | - Real time Operating Systems | - Parallel Computer Architecture |
| - Computer Architecture    | - Dynamic Compilation         | - Multicore Computing            |
| - Distributed Systems      | - Microarchitecture           | - Mobile Computing               |
| - Machine Learning         | - Compilers                   |                                  |

## **TECHNICAL STRENGTHS**

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|---|---|
| <b>Programming/Scripting</b>            | C, C++, Java, MPI, CUDA, Cilk, pThreads, python |
| <b>Testing Platforms and simulators</b> | Pin, Trace32, Veloce, GPGPUSim                  |
| <b>Protocols</b>                        | USB, PCIe, eMMC/SD, NAND, SPI, HSIC, NOCs       |
| <b>Processor Architectures</b>          | ARM Cortex A/M for v8, Hexagon, Intel x86       |